a) modeling a small signal electrical equivalent circuit for said semiconductor device which includes a plurality of electrical circuit elements defining a small signal model, said small signal equivalent circuit based in part on one or more real process parameters;

A1

b) deriving said electrical circuit elements at least in part from a small signal excitation analysis of at least one of the intrinsic charge and electrical field characteristics of said semiconductor device.

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4. (Amended) The method as recited in claim 1, wherein said real process parameters include at least one of: gate length recess, etch depth, recess undercut dimensions and passivation nitrite thickness.

A2

5. (Amended) The method as recited in claim 1, wherein step (b) includes the step of:

determining the relationships between one or more conduction band offsets and electrical permitivities and the material composition for the materials in the semiconductor device.

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8. (Amended) The method as recited in claim 5, further including step (e); determining the electron transport characteristics of any bulk materials in the semiconductor device.

A3

9. (Amended) The method as recited in claim 8, further including step (f); determining an undepleted linear channel mobility.

a3

10. (Amended) The method as recited in claim 9, wherein step (f) is determined by material characterization.

13. (Amended) A method of modeling a semiconductor device comprising the steps of:

(a) modeling a small signal on an electrical equivalent circuit for said semiconductor device with a plurality of electrical circuit elements defining a small signal model;

a4

deriving said electrical circuit elements from a small signal excitation analysis of the intrinsic charge within said semiconductor device by determining the relationships between one or more of the conduction band offsets and electrical permitivities and the material composition for the materials in the semiconductor device;

determining the electron transport characteristics of any bulk materials in the semiconductor device;

determining an undepleted linear channel mobility;

forming semiconductor physical equations with empirical terms for modeling one or more of the following characteristics: fundamental-charge control physics for sheet charge in an active channel as controlled by a gate terminal voltage; average centroid position of the sheet charge within the active channel width; position of charge partitioning boundaries as a function of gate, drain and source terminal voltages; bias dependence of linear channel mobility and surface depleted regions; bias dependence of a velocity saturating electric field of the channel; saturated electron velocity; electrical conductance within the linear region of the channel, under the gate; electrical conductance within the source and drain access regions.

16. The method as recited in claim 1, wherein said semiconductor device model is based at least in part as a function of one or more of: conduction band offsets; electrical permitivities; and material composition of the epi stack.

17. The method as recited in claim 4, wherein said real process parameters further include: gate-source recess, gate-drain recess, gate-source spacing and source-drain spacing.

18. The method as recited in claim 1, wherein said semiconductor device is a high electron mobility transistor (HEMT).

19. The method as recited in claim 1, wherein said semiconductor device is a field effect transistor (FET).